800mA, Single-Input, Single Cell Li-Ion Battery Solar Charger

Check for Samples: bq24210

FEATURES

- **Input Voltage Dynamic Power Management Feature (VBUS_DPM)**
- **Selectable Battery Tracking Mode to Maximize the Charge Rate from Solar Panel Using DPM Feature**
- **Load Mode to Support Loads Connected at VBUS Pin**
- **20V Input Rating, with Over-Voltage Protection (OVP)**
- **1% Battery Voltage Regulation Accuracy**
- **Up to 800mA Charge Current with 10% Charge Current Accuracy**
- **Thermal Regulation Protection for Output Current Control**
- **Low Battery Leakage Current**
- **BAT Short-Circuit Protection**
- **NTC Input Monitoring**
- **Built-In Safety Timer With Reset Control**
- **Status Indication – Charging/Power Present**
- **Available in Small 2mm × 3mm SON-10 Package**

APPLICATIONS

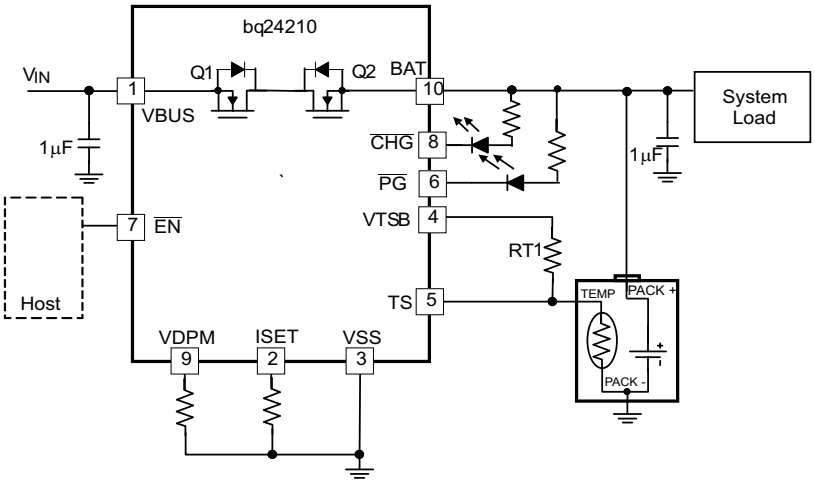
- **Smart Phones**
- **PDAs**
- **MP3 Players**
- **Low-Power Handheld Devices**
- **Auxiliary Solar Chargers**

DESCRIPTION

The bq24210 is a highly integrated Li-ion linear charger targeted at space-limited portable applications. The high input voltage range with input over-voltage protection supports low-cost unregulated adapters. The input voltage regulation loop with programmable input voltage regulation threshold make it suitable for charging from alternative power sources, such as solar panel or inductive charging pad.

The IC has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

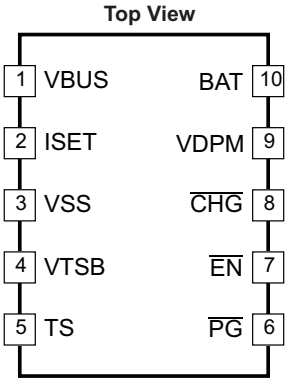
DESCRIPTION (CONTINUED)

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination function. The charge current value is programmable via an external resistor.

Furthermore, the IC has a Load Mode that connects the battery to VBUS pin with current limiting function to prevent over load. To use Load Mode, the charging source would be removed from the VBUS pin. Then a load can be placed on VBUS pin and it will be near the VBAT pin voltage.

PIN CONFIGURATION

Figure 1. DQC PACKAGE



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VBUS	1	I/O	For Charging Mode, input for charging source, connect to external DC supply (ie, Solar Panel, Inductive charging PAD, or Wall Adapter) For Load Mode, output for current limited battery voltage. Expected range of bypass capacitors 1µF to 10µF, connected from VBUS to VSS.
BAT	10	I/O	Battery Connection. System Load may be connected. Expected range of bypass capacitors 1µF to 10µF, connected from BAT to VSS.
VDPM	9	I	Programs the input voltage regulation threshold. Expected range of programming resistor is 1kΩ to 10 kΩ, connected from VDPM to VSS. When VDPM is floating, the VIN DPM loop operates in battery tracking mode, and the VIN DPM threshold is BAT+100mV (BAT>3.6V) or 3.7V (BAT≤3.6V) in this case. VIN DPM threshold should be programmed higher than battery voltage to ensure proper operation.
ISET	2	I	Programs the Fast-charge current setting. External resistor from ISET to VSS defines fast charge current value.
$\overline{PG}$	6	O	Power Present indication. LOW (FET ON) When input voltage is in normal range (VBUS>BAT and VBUS>UVLO), High impedance (open drain FET OFF) in other cases.
TS	5	I	Temperature sense pin, connected to NTC Thermistor in the battery pack. Pulling High puts part in Limited Power charging mode. Must not be left floating.
VSS	3	–	Ground terminal
$\overline{CHG}$	8	O	Charge Status indication, Low (FET ON) indicates charging, and High impedance (open drain FET OFF) in other cases
$\overline{EN}$	7	I	Chip enable control. Low to enable Charge or Load Mode, and High to enable Suspend mode.
VTSB	4	O	TS bias reference voltage pin, regulated output. No external capacitor is required from VTSB to VSS. Only enabled during charge.
Thermal PAD and Package	–	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

TYPICAL APPLICATION CIRCUIT: bq24210

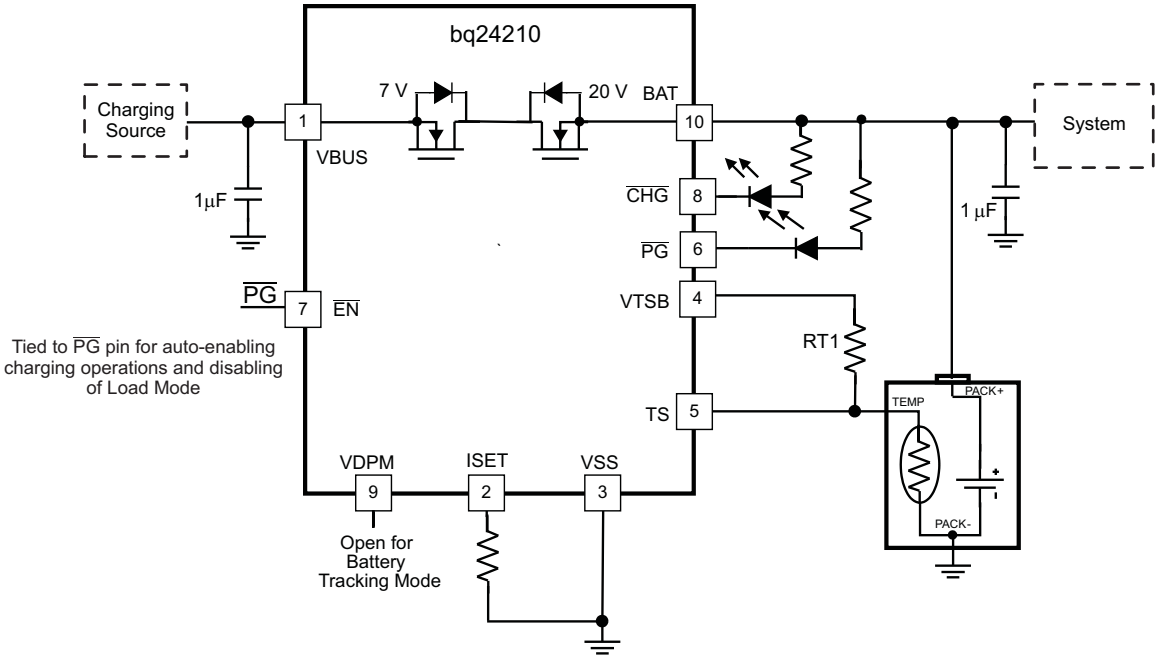


Figure 2. Typical System Schematic

ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)

		VALUE	UNIT
Input Voltage	VBUS (with respect to VSS)	–0.3 to 20	V
	BAT (with respect to VSS)	–0.3 to 7	
	VDPM, VTSB, ISET, TS, $\overline{EN}$, $\overline{CHG}$, $\overline{PG}$ (with respect to VSS)	–0.3 to 7	
Input Current	VBUS	1.25	A
Output Current (Continuous)	BAT	1.25	A
Output Sink Current	$\overline{CHG}$, $\overline{PG}$	15	mA
Junction temperature, T_J		–40 to 150	°C
Storage temperature, T_{STG}		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		bq24210 SON-10 PIN	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	60.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.1	
θ_{JB}	Junction-to-board thermal resistance	22.2	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	22.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	4.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNITS
VBUS	Voltage range	3.5	18	V
	Operating voltage range, Restricted by UVLO and OVP	3.5	7.0	
IBUS	Input current, VBUS pin		0.8	A
I_{BAT}	Current, BAT pin		0.8	A
T_J	Junction Temperature	0	125	°C
R_{VDPM}	Programs input voltage regulation Thresholds	1k	10k	Ω
R_{ISET}	Fast-charge current programming resistor	675	10.8K	Ω
V_{TS}	Voltage across NTC Thermistor for charging	12	57	%VTSB
C_{BAT}	By-pass capacitor on BAT pin	1	10	µF
C_{VBUS}	By-pass capacitor on VBUS pin	1	10	µF
C_{VTSB}	By-pass capacitor on VTSB pin		0.1	µF

ELECTRICAL CHARACTERISTICS

Over junction temperature range 0°C ≤ T_J ≤ 125°C, VBUS=5V, Charge mode ($\overline{EN}$ = Low) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{UVLO}	Under-voltage lock-out Exit	VBUS: 0V → 4V		3.15	3.3	3.45	V
V_{HYS_UVLO}	Hysteresis on V_{UVLO} Falling	VBUS: 4V→0V, V_{UVLO_FALL} = V_{UVLO}–$V_{HYS-UVLO}$		175	227	280	mV
V_{BUS-DT}	Input Power Good detection threshold VBUS above BAT	(Input power good if VBUS > BAT + V_{BUS-DT}); BAT = 3.6V, VBUS: 3.5V → 4V		150	200	250	mV
$V_{HYS-VBUSDT}$	Hysteresis on V_{BUS-DT} Falling	BAT = 3.6V, VBUS: 4V → 3.5V			250		mV
$t_{DGL(PG\_PWR)}$	Deglitch time on exiting sleep	Time measured from VBUS: 0V → 5V 1µs rise-time to $\overline{PG}$ = Low, BAT=3.6V			90		µs
$t_{DGL(PG\_NO-PWR)}$	Deglitch time on $V_{HYS-VBUSDT}$ power down. Same as entering sleep.	Time measured from VBUS: 5V → 3.2V 1µs fall-time to $\overline{PG}$ = Open Circuit			29		ms
V_{OVP}	Input over-voltage protection threshold	VBUS: 5V → 8V		7.3	7.5	7.7	V
$V_{HYS-OVP}$	Hysteresis on OVP	VBUS: 11V → 5V			200		mV
$t_{BLK(OVP)}$	Input over-voltage blanking time	VBUS: 5V → 12V			113		µs
$t_{DGL(PG\_OVP)}$	Deglitch time exiting OVP	Time measured from VBUS: 12V → 5V 1µs fall-time to $\overline{PG}$ = Low			5		ms
$V_{BUS-DPM}$	Input voltage regulation threshold. Restricts Iout at $VBUS_{\_DPM}$	Programmable, the programming resistor at VDPM pin R_{VDPM} = 1kΩ		3.55	3.65	3.75	V
		Programmable, the programming resistor at VDPM pin R_{VDPM} = 10kΩ		4.8	5	5.1	
$KVBUS_{\_DPM}$	Term Factor	BAT > V_{LOWV}, VBUS = 5V, R_{VDPM} = 1k to 10kΩ; R_{VDPM} = $KVBUS_{\_DPM}$ × ($VBUS_{\_DPM}$–$VBUS_{\_DPM\_1}$)		0.135	0.15	0.165	V/KΩ
$VBUS_{\_DPM\_1}$	Initial voltage for VBUS_DPM threshold setting	BAT > V_{LOWV}, VBUS = 5V, R_{VDPM} = 1k to 10kΩ		3.41	3.5	3.59	V
$VBUS_{\_DPM\_0}$	VBUS_DPM threshold when VDPM is shorted to VSS	BAT > V_{LOWV}, VBUS = 5V, R_{VDPM} < 500Ω			3.65		V
$IVBUS_{\_DPM}$	Current for programming $VBUS_{\_DPM}$				75		µA
V_{TRK}	Battery voltage tracking threshold for VBUS DPM loop	VDPM pin Float (open circuit, R_{TS} > 500kΩ), BAT rising	BAT ≤ 3.6V	3.65	3.7	3.75	V
			BAT > 3.6V	BAT +0.07	BAT +0.10	BAT +0.145	
V_{TRK_HYS}	Hysteresis for V_{TRK}	BAT falling			60		mV
V_{BUS_CHG}	Input voltage to enable $\overline{CHG}$ pin, VBUS-V_{BUS_DPM} or VBUS-V_{TRK}	$\overline{EN}$=LOW, VBUS rising above VIN DPM threshold			80		mV
$V_{BUS\_CHG\_HYS}$	Hysteresis for V_{BUS_CHG}	$\overline{EN}$=LOW, VBUS falling			160		mV
t_{DGL_CHG}	Deglitch time for $\overline{CHG}$ pin status change				5		mS
ISET SHORT CIRCUIT TEST							
R_{ISET_MAX}	Highest Resistor value considered a fault (short). Monitored for Iout>90mA	Riset: 600 Ω → 250 Ω, Iout latches off. Cycle power to Reset. Fault range >1.10A		200	250	300	Ω
$t_{DGL-SHORT}$	Deglitch time transition from ISET Short to Iout Disable	Clear fault by cycling IN or $\overline{CHGEN}$			1		ms
I_{OUT_CL}	Maximum OUT current limit regulation (Clamp)			0.95		1.4	A
BATTERY SHORT PROTECTION							
$I_{BAT(SC)}$	Source current out BAT pin during short-circuit detection			13	17	21	mA
$BAT_{(SC)}$	BAT pin short-circuit detection threshold/ Pre-Charge Threshold	BAT:3V → 0.5V, no deglitch		0.75	0.8	0.85	V
$BAT_{(SC-HYS)}$	BAT pin Short Hysteresis	Recovery → $BAT_{(SC)}$ + $BAT_{(SC-HYS)}$; Rising, no Deglitch			77		mV

ELECTRICAL CHARACTERISTICS

Over junction temperature range 0°C ≤ T_J ≤ 125°C, VBUS = 5V, Charge mode ($\overline{EN}$ = Low) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
$I_{OUT(DONE)}$	BAT pin current, charging terminated	$\overline{EN}$=Low, VBUS = 6V, Terminated			9	µA
$I_{OUT(STDBY)}$	Suspend current into BAT pin	$\overline{EN}$=High, VBUS =0V, BAT = 4.2 V			5	µA
$IBUS_{(STDBY)}$	Suspend current into VBUS pin	$\overline{EN}$=High, VBUS ≤ 6V		100	175	µA
I_{CC}	Active supply current, VBUS pin	No load on VTSB pin, $\overline{EN}$=Low, VBUS = 6V, no load on BAT pin, BAT > $V_{O(REG)}$, IC enabled		0.8	1.2	mA
I_{CC_REV}	Active supply current, BAT pin in Load Mode	$\overline{EN}$ = Low, BAT = 4V, no load on VBUS pin		50	80	µA
BATTERY CHARGER FAST-CHARGE						
$V_{O(REG)}$	Battery regulation voltage	VBUS = 5.5V, I_{OUT} = 25 mA, (V_{TS_0C}<V_{TS}<V_{TS_45C})	4.16	4.20	4.23	V
$V_{O\_HT(REG)}$	Battery hot regulation Voltage	VBUS = 5.5V, I_{OUT} = 25 mA, (V_{TS_45C}<V_{TS}<V_{TS_60C})	4.02	4.06	4.1	
I_{OUT}	Programmed output "fast charge" current range	$V_{O(REG)}$ > BAT > V_{LOWV}, VBUS = 5V, R_{ISET} = 469 to 7.5kΩ	50		800	mA
$V_{DO(IN-OUT)}$	Drop-Out, VBUS – BAT	Adjust VBUS down until I_{OUT} = 0.5A, BAT = 4.15 V, R_{ISET} = 675, T_J <100°C.		250	400	mV
I_{OUT}	Output "fast charge" formula	$V_{O(REG)}$ > BAT > V_{LOWV}, VBUS = 5V		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor	R_{ISET} = K_{ISET} /I_{OUT}; 250 mA ≤ I_{OUT} < 800 mA	373	390	407	AΩ
		R_{ISET} = K_{ISET} /I_{OUT}; 50mA ≤ ICHG < 250 mA	375	395	416	
		R_{ISET} = K_{ISET} /I_{OUT}; 10 < ICHG < 50 mA	320	400	490	
PRE-CHARGE – INTERNALLY SET						
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			100		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			32		ms
$I_{PRE-CHG}$	Pre-charge current, Internally set	BAT < V_{LOWV}, ICHG ≥ 250 mA	18	20	22	% IOUT
TERMINATION – INTERNALLY SET						
I_{TERM}	Termination current, Internally set	ICHG ≥ 250 mA	8	10	12	% ICHG
$t_{DGL(TERM)}$	Deglitch time, termination detected			29		ms
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold- normal temp	V_{TS_0C}<V_{TS}<V_{TS_45C}, BAT: 4.2V → V_{RCH}	$V_{O(REG)}$ –0.120	$V_{O(REG)}$ –0.095	$V_{O(REG)}$ –0.070	V
	Recharge detection threshold-hot temp	V_{TS_45C}<V_{TS}<V_{TS_60C}, BAT: 4.15V → V_{RCH}	$VO_{(REG)}$ –0.130	$V_{O(REG)}$ –0.105	$V_{O(REG)}$ –0.80	V
$t_{DGL1(RCH)}$	Deglitch time, recharge threshold detected	V_{TS_0C}<V_{TS}<V_{TS_45C}, BAT: 4.25V → 3.5V in 1µS ; $t_{DGL(RCH)}$ is time to ISET ramp		29		ms
$t_{DGL2(RCH)}$	Deglitch time, recharge threshold in BAT_Detect mode	V_{TS_0C}<V_{TS}<V_{TS_45C}, BAT: 3.5V inserted; $t_{DGL(RCH)}$ is time to ISET ramp		3.6		ms
BATTERY DETECTION ROUTINE						
V_{REG_BD}	BAT Reduced regulation during battery detect	V_{TS_0C}<V_{TS}<V_{TS_45C}, Battery present	$V_{O(REG)}$ –0.45	$V_{O(REG)}$ –0.4	$V_{O(REG)}$ –0.35	V
V_{BD_SINK}	Sink current during V_{REG_BD}	V_{TS_0C}<V_{TS}<V_{TS_45C}, Battery present	5	7	9	mA
$t_{DGL1(HI/LOW\_REG)}$	Regulation time at V_{REG} or V_{REG_BD}	V_{TS_0C}<V_{TS}<V_{TS_45C}, Battery present		25		ms
V_{BD_HI}	High battery detection threshold	V_{TS_0C}<V_{TS}<V_{TS_45C}, Battery present	$V_{O(REG)}$ –0.158	$V_{O(REG)}$ –0.108	$V_{O(REG)}$ –0.058	V
V_{BD_LO}	Low battery detection threshold	V_{TS_0C}<V_{TS}<V_{TS_45C}, Battery present	V_{REG_BD} +0.05	V_{REG_BD} +0.1	V_{REG_BD} +0.15	V
BATTERY CHARGING TIMERS AND FAULT TIMERS						
t_{PRECHG}	Pre-charge safety timer value	Restarts when entering Pre-charge; Always enabled when in pre-charge. V_{TS}<$V_{SM(TS)}$	1700	1940	2250	s
t_{MAXCH}	Charge safety timer value	Clears fault or resets at UVLO, $\overline{EN}$ disable, BAT Short, exiting LOWV and Refresh	34000	38800	45000	s

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C, VBUS = 5V, Charge mode ($\overline{EN}$ = Low) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{MAXTERM}$	Termination timer in Limited Power Charge mode	Limited Power Charge mode, terminate charge when VIN DPM active, normal termination conditions met and this termer expires	6800	7760	9000	s
BATTERY-PACK NTC MONITOR						
VTSB	TS Bias Voltage	I_{VTSB} < 1 mA	2	2.2	2.4	V
I_{VTSB} (Min)	Maximum current from TS-bias pin (short circuit protection)				1	mA
C_{VTSB}	Optional capacitance for ESD				0.1	µF
C_{TS}	Optional capacitance for ESD			0.22		µF
V_{0C}				57		%VTSB
$V_{0C-Hyst}$	Hysteresis on 0C comparator			1		%VTSB
V_{10C}				46		%VTSB
$V_{10C-Hyst}$	Hysteresis on 10C comparator			1		%VTSB
V_{45C}				18.6		%VTSB
$V_{45C-Hyst}$	Hysteresis on 45C comparator			1		%VTSB
V_{60C}				12		%VTSB
$V_{60C-Hyst}$	Hysteresis on 60C comparator			1		%VTSB
$t_{DGL(TS\_10C)}$	Deglitch for TS thresholds: 10C	Normal to cold operation: V_{TS}: 30% → 50% VTSB		50		ms
		Cold to Normal operation: V_{TS}: 50% → 30% VTSB		12		
$t_{DGL(TS)}$	Deglitch for TS thresholds: 10/45/60C	Battery charging		30		ms
$V_{LP(TS)}$	Limited Power Charge mode threshold - Enter	V_{TS}: 0.4VTSB → 0.9VTSB;	75	80	85	%VTSB
$V_{HYS-LP(TS)}$	Hysteresis exiting Limited Power Charge mode	V_{TS}: 1.7V → 0.5V;		5		
$t_{DGL(LDO)}$	Deglitch exit Limited Power Charge mode between states	Battery charging		57		ms
	Deglitch enter Limited Power Charge mode between states			8		µs
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON $\overline{EN}$						
V_{IL}	Logic LOW input voltage	Sink 8 µA			0.4	V
V_{IH}	Logic HIGH input voltage	Source 8 µA	1.4			V
I_{IL}	Sink current required for LO		2		10.5	µA
I_{IH}	Source current required for HI		0.8		2	µA
LOGIC LEVELS ON $\overline{CHG}$ AND $\overline{PG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V
I_{LEAK}	Leakage current into IC	Vchg = 5 V, VPG = 5 V			1	µA
LOAD MODE ($\overline{EN}$=LOW)						
$BAT_{\_REV\_ST}$	Minimum voltage for Load Mode		2.8	3.0	3.2	V
$V_{DO(BAT-VBUS)}$	Drop-Out, V(BAT) – V(VBUS)	Adjust VBUS down until I(VBUS) = 0.1A, BAT = 4.15V, T_J <100°C.		200	320	mV
V_{BUS-LM}	Load mode exiting threshold (VBUS above BAT)	BAT = 3.6V, VBUS: rising 3V → 4V	–100	–50	0	mV
$V_{HYS-VBUSLM}$	Hysteresis on V_{BUS-LM} falling	BAT = 3.6 V, VBUS: 4V → 3V		150		mV
$t_{DGL(LM\_Exit)}$	Deglitch time on exiting load mode			100		mS
$t_{DGL(LM-Enter)}$	Deglitch time on $V_{HYS-VBUSLM}$ same as entering load mode			5		µs
I_{LM_MIN}	The minimum load current to keep IC in load mode	During load mode	0.3	1.8	3.1	mA
I_{REV_LIMIT}	Initial current limit in load mode for blanking time $t_{REV\_LIMIT\_BLK}$	BAT = 3.6V	130	170	215	mA

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C, VBUS = 5V, Charge mode ($\overline{EN}$ = Low) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{REV\_LIMIT\_BLK}$	Blanking time for initial current limit			200		ms
$I_{REV\_LIMIT\_BK}$	Reverse load mode current limit after the initial blanking time		40	55	70	mA
$t_{REV\_LIMIT\_REC}$	Delay time to set load current limit back to I_{REV_LIMIT}	Reverse current drops from 100% to 30% of $I_{REV\_LIMIT\_BK}$		200		ms

SIMPLIFIED FUNCTION BLOCK DIAGRAM

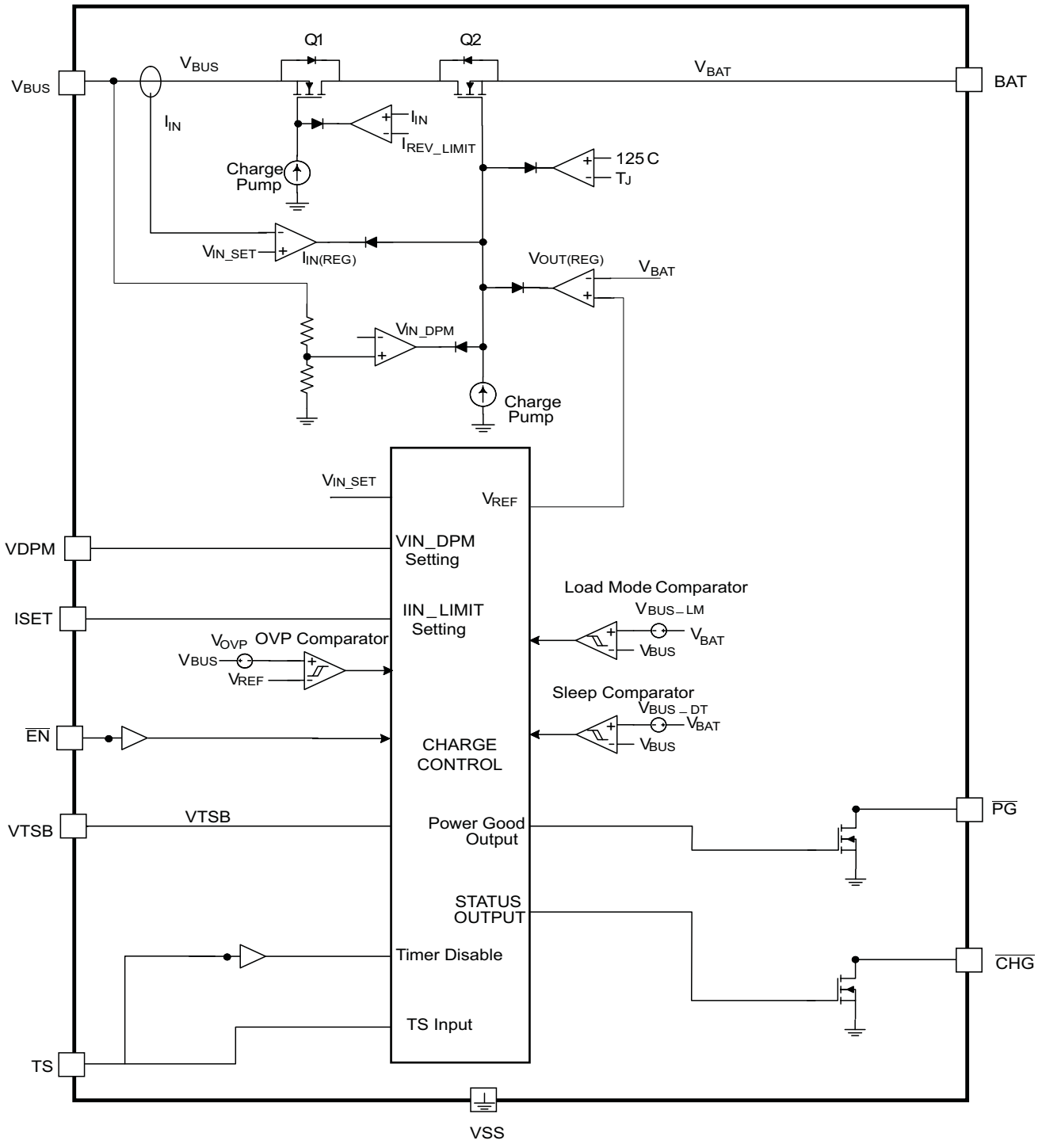


Figure 3. Functional Block Diagram

DETAILED FUNCTIONAL DESCRIPTION

OVERVIEW

The bq24210 is a highly integrated 2x3 mm^2 single cell Li-Ion charger with bi-directional power flow capability. Depending on the status of control pins and source conditions, the IC can operate in several modes: Sleep, Charge, Load, and Suspend mode.

At power up (VBUS or BAT ramps up, or $\overline{EN}$ pin changes status), the IC performs the operation mode detection automatically. Depending on the VBUS and BAT levels, the IC enters sleep, charge, load, or suspend mode.

In charge mode, the charger has three phases of charging: Pre-charge to recondition a full discharged battery, fast-charge constant current to supply the buck charge safely and voltage regulation to safely reach full capacity, as shown in Figure 4. The charge operating mode is very flexible, allowing programming of the fast-charge current, and input voltage regulation threshold. The programmable input voltage regulation threshold makes the IC compatible with many alternative power sources, such as solar panel or inductive charging pad.

In Load Mode, the IC connects the battery voltage to the input pin (VBUS pin) through the back to back FET (Q1 and Q2) to power the load connected at VBUS pin. The load current is limited to provide over load protection.

In sleep mode, Q2 is OFF and the IC standby current is reduced to I_{CC_REV}.

In suspend mode, the IC turns off both Q1 and Q2, and no charging or reverse conduction is allowed.

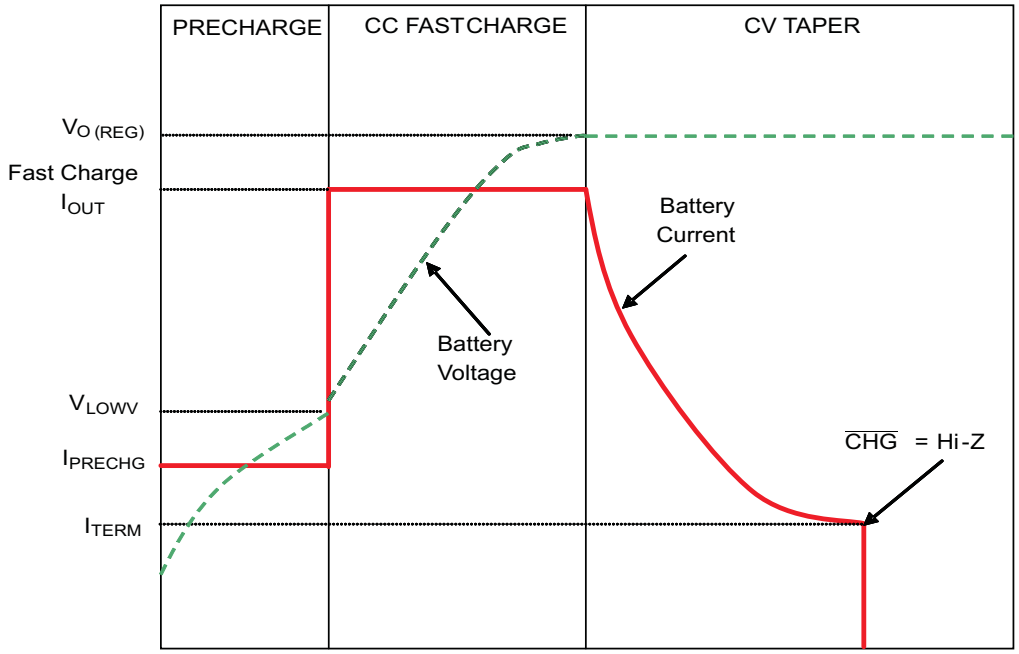


Figure 4. Charge Profile

OPERATION MODE DETECTION AND TRANSITION

On power up (VBUS or BAT ramps up, or $\overline{EN}$ pin changes status), the IC performs operation mode detection to identify the operation mode based on the VBUS voltage, battery voltage, load current, and control pin status.

Two comparators are needed for the detection, Load Mode comparator and Sleep Mode comparator.

When VBUS falls below the lower limit of the Load Mode comparator, the IC goes to Load Mode; when VBUS is above the upper limit of the Sleep comparator, the IC goes to Charge Mode, as shown in Figure 5.

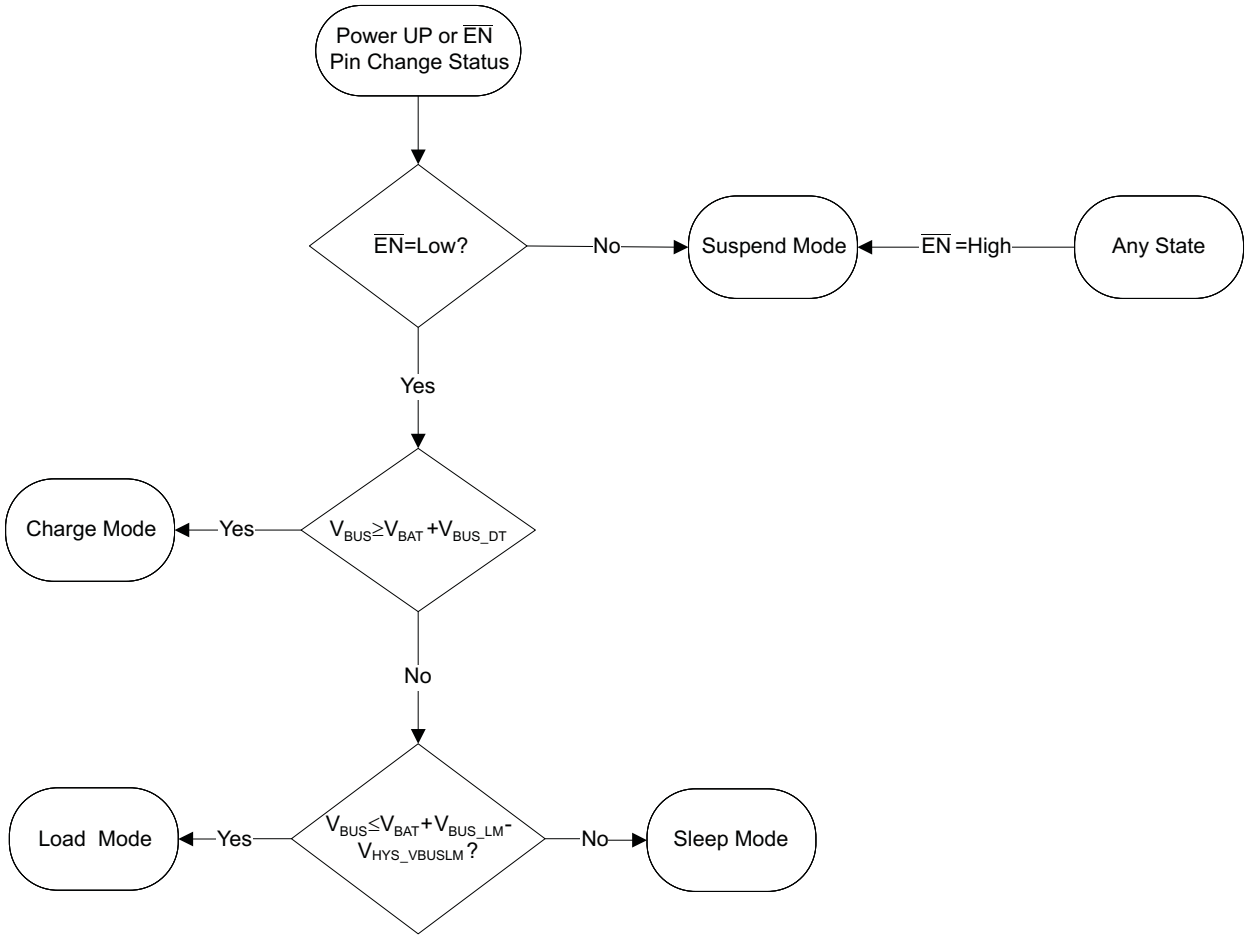


Figure 5. Operation Mode Detection Flow Chart

During Load Mode, when VBUS is above upper limit of Load Mode and the load current is below the minimum load current (I_{LM_MIN}), the IC stays in Load Mode for a deglitch time of 100mS and then goes to sleep mode.

If VBUS is above the upper limit of the Sleep comparator during this period, after 45µs deglitch time, the IC stops Load Mode and goes into the Charge Mode. The maximum current to the battery is limited by the FET RDSon during this transition.

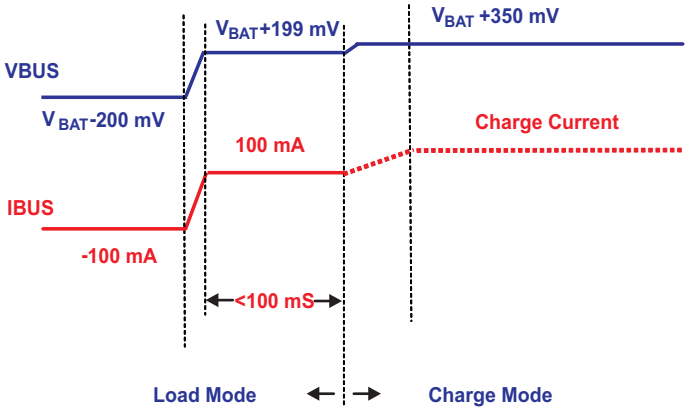


Figure 6. Sleep Comparator Operation

During Charge Mode, if VBUS falls to the lower limit of Sleep comparator, the IC goes to Sleep Mode after a deglitch time of 32 mS. If VBUS falls faster than 32 ms to below the lower limit of Load Mode comparator, the IC goes to Load Mode after a deglitch time of 32ms, as shown in Figure 7.

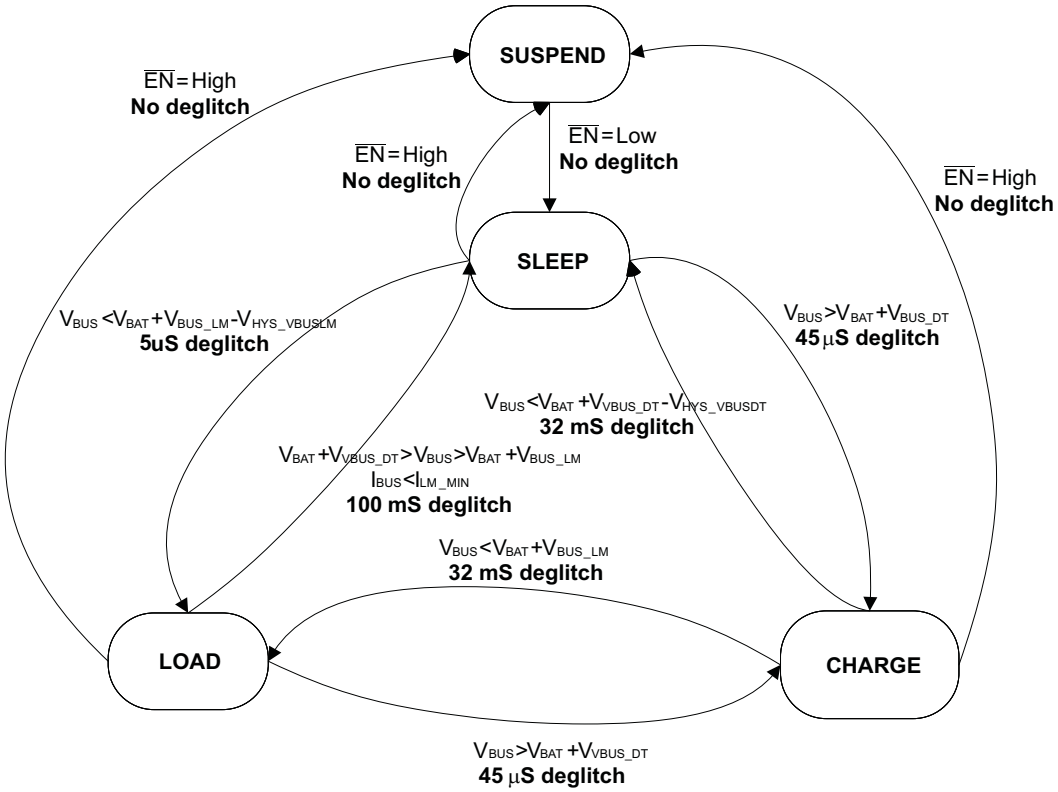


Figure 7. Operation Mode Transition Diagram

In Load Mode, if the load is higher than I_{LM_MIN}, or the voltage at VBUS pin is lower than upper limit of Load Mode comparator, Load Mode is continuous.

If the load is smaller than I_{LM_MIN} in Load Mode, and VBUS is higher than the upper limit, then the IC goes to Sleep Mode after deglitch time of 100mS. In Sleep Mode, once VBUS drops lower than the lower limits of the Load Mode comparator, the IC goes to Load Mode again. In this case, the above process repeats, and IC keeps changing operations mode (between Sleep Mode and Load Mode). The mode change frequency is less than 10Hz, and VBUS has a ripple of 150mV.

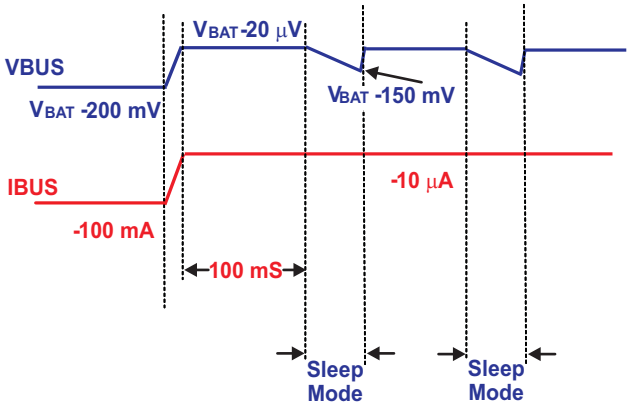


Figure 8. Load Mode Operation

CHARGE MODE

Power-Down or Under-Voltage Lockout (UVLO)

The IC is in power down mode if the VBUS and BAT pin voltages are both less than UVLO. The part is considered "dead" and all the pins are high impedance. Once the VBUS voltage rises above the UVLO threshold the IC enters Sleep Mode or an active mode depending on control pin status and the BAT pin (battery) voltage.

Power-Up

The IC is alive after the VBUS or BAT voltage ramps above UVLO (see Sleep Mode), the IC resets all logic and timers, and starts to perform many of the continuous monitoring routines. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the safety timer, enables the CHG pin, and starts the normal charge routine.

Sleep Mode

If the VBUS pin voltage is below the BAT voltage and above the UVLO threshold, the charge current is disabled, the safety timer counting pauses (not reset) and the $\overline{PG}$ and $\overline{CHG}$ pins are high impedance. As the input voltage rises and the charger exits Sleep Mode, the $\overline{PG}$ pin goes low, the safety timer continues to count, charge is enabled, and the $\overline{CHG}$ pin remains high impedance until current flows out the BAT pin.

New Charge Cycle

A new charge cycle is started when a good power source is applied, when performing a charge disable/enable ($\overline{EN}$), when exiting Limited Power Charge Mode (LPCM), when detecting a battery insertion, or when the BAT voltage dropping below the VRCH threshold. The $\overline{CHG}$ pin is active low only during the first charge cycle, therefore exiting LPCM or dropping below VRCH will not turn on the $\overline{CHG}$ pin FET, if the $\overline{CHG}$ pin is already high impedance.

Overvoltage-Protection (OVP) – Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer ends and the $\overline{CHG}$ and $\overline{PG}$ pins go to a high impedance state. Once the overvoltage returns to a normal voltage and after a deglitch time of $t_{DGL(PG\_OVP)}$, the $\overline{PG}$ pin goes low, timer continues, charge continues, and the $\overline{CHG}$ pin goes low after a 25ms deglitch.

Power Good Indication ($\overline{PG}$)

After a source is applied to VBUS and the voltage rises above the UVLO and sleep thresholds (VBUS>BAT+V_{BUS-DT}) and VIN DPM threshold (V_{BUS_DPM} or V_{TRK}), but is less than OVP (VBUS<V_{OVP}), then the $\overline{PG}$ FET turns on and provides a low impedance path to ground. The EN pin state does not affect this functionality.

$\overline{CHG}$ Pin Indication

The charge pin has an internal open drain FET which is on (pulls down to V_{SS}) during the first charge only (unless TS pin is tied to VTSB pin) and is turned off once the battery reaches voltage regulation and the charge current tapers to the internally set termination threshold.

The charge pin is high impedance in Sleep Mode and OVP (if $\overline{PG}$ is high impedance) and return to its previous state once the condition is removed.

Cycling input power, toggling $\overline{EN}$ pin, or releasing or entering pre-charge mode causes the $\overline{CHG}$ pin to go low if power is good and a discharged battery is attached. This is considered the start of a first charge cycle.

$\overline{CHG}$ and $\overline{PG}$ LED Pull-Up Source

For host monitoring, a pull-up resistor is used between the *STATUS* pin and the V_{CC} of the host. For a visual indication a resistor in series with an LED is connected between the *STATUS* pin and a power source. If the $\overline{CHG}$ or $\overline{PG}$ source is capable of exceeding 7V, a 6.2V zener should be used to clamp the voltage. If the source is the BAT pin, note that as the battery changes voltage, the brightness of the LEDs vary.

CHARGING STATE	$\overline{CHG}$ FET/LED (VTS< $V_{LP(TS)}$)	$\overline{CHG}$ FET/LED (VTS> $V_{LP(TS)}$)
1st Charge	ON	ON
Refresh Charge	OFF	ON
OVP		OFF
Sleep		OFF
TEMP Fault	ON for 1st Charge	ON
Charge when BAT< $BAT_{(SC)}$	OFF	ON

INPUT POWER GOOD STATE	$\overline{PG}$ FET/LED
Normal Input ($BAT+VBUS_{\_DT}<VBUS<V_{OVP}$) and ($VBUS_{DPM}<V_{BUS}<V_{OVP}$)	ON
UVLO	OFF
Sleep Mode	
OVP mode	
$\overline{PG}$ is independent of chip disable	

Input Voltage Based Dynamic Power Management (VBUS-DPM)

The VBUS-DPM feature is used to detect an input source voltage that is folding reaching its current limit due to excessive load and causing the voltage to reduce.. When the input voltage drops to the VBUS-DPM threshold the internal pass FET reduces the current until there is no further drop in voltage at the input. This prevents a source with voltage less than $VBUS_{\_DPM}$ to power the BAT pin. This unique feature makes the IC work well with current limited power sources, such as solar panels or inductive changing pads. This is also an added safety feature that helps protect the source from excessive loads.

BAT

The charger's BAT pin provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system or charge just the battery assuming the loads do not exceed the available current. The BAT pin is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output voltage will drop unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

VDPM

An external resistor is used to program the $VBUS_{\_DPM}$. The programming resistor, R_{VDPM} is dictated by the following equation:

$$R_{VDPM} = (VBUS_{\_DPM} – VBUS_{\_DPM\_1})/KVBUS_{\_DPM}$$

Where:

$VBUS_{\_DPM}$ is the desired input voltage regulation voltage threshold;
$VBUS_{\_DPM\_1}$ is the built in offset threshold, typically 3.5V
K_{VBUS_DPM} is a gain factor found in the electrical specification.

If VDPM pin is shorted to VSS, the $VBUS_{\_DPM}$ is set to typically 3.65V.

If the VDPM pin is floated (open circuit), the IC operates in Battery Tracking Mode. In this case, VBUS DPM threshold is internally set as V_{TRK}, which is typically BAT+100mV (BAT>3.65V) or 3.75V (BAT≤3.4V).

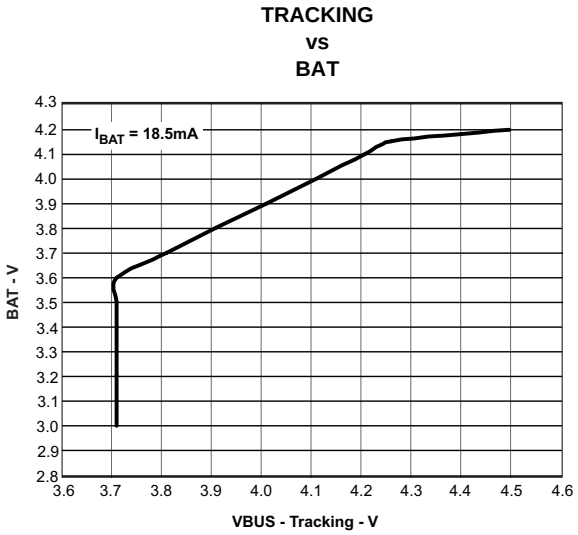


Figure 9.

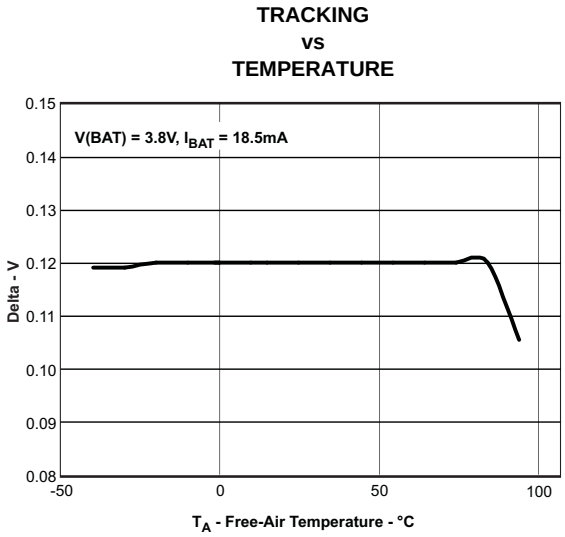


Figure 10.

ISET

An external resistor is used to program the output current (50 to 800mA) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} \div I_{OUT}$$

Where:

I_{OUT} is the desired fast charge current in amps;
K_{ISET} is a gain factor found in the electrical specification, typically 395 AΩ

The ISET resistor is short protected and will detect a resistance lower than R_{ISET_MAX}. The detection requires at least 80mA of output current. If a *short* is detected, then the IC will latch off and can only be reset by cycling the power. The BAT current is internally clamped to a maximum current I_{OUT_CL} which is independent of the ISET short detection circuitry.

Pre-Charge and Termination

The termination and pre-charge current are internally set at 10% and 20% of fast charge current I(BAT), respectively. The pre-charge-to-fast-charge, V_{lowv} threshold is set to 2.5V.

TS

The TS pin is designed to be compatible with the JEITA temperature standard for Li-Ion batteries. There are four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C, the charge current level is cut in half and if between 45°C and 60°C, the regulation voltage is reduced to 4.1Vmax.

The voltage based TS sensing is used due to the flexibility to be compatible with different NTCs. VTSB is used as the voltage reference for TS sensing, and two external TS voltage divider (RT1 and RTH) are used to set the targeted temperature threshold. Above 60°C or below 0°C the charge is disabled.

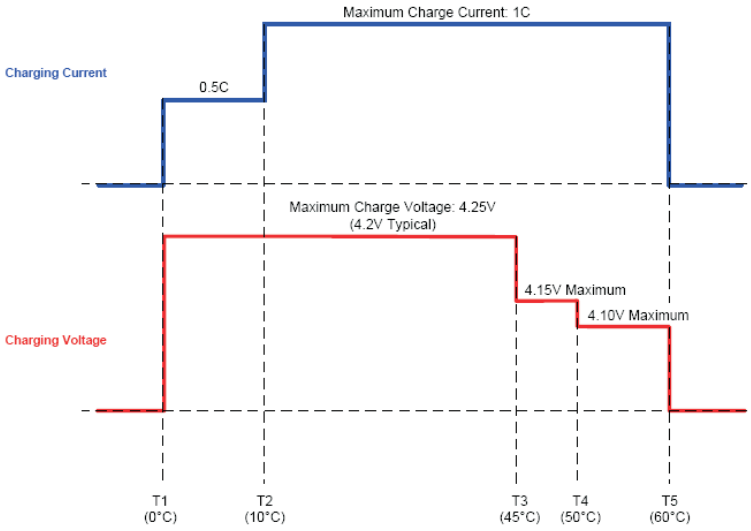


Figure 11. Charge JEITA Profile

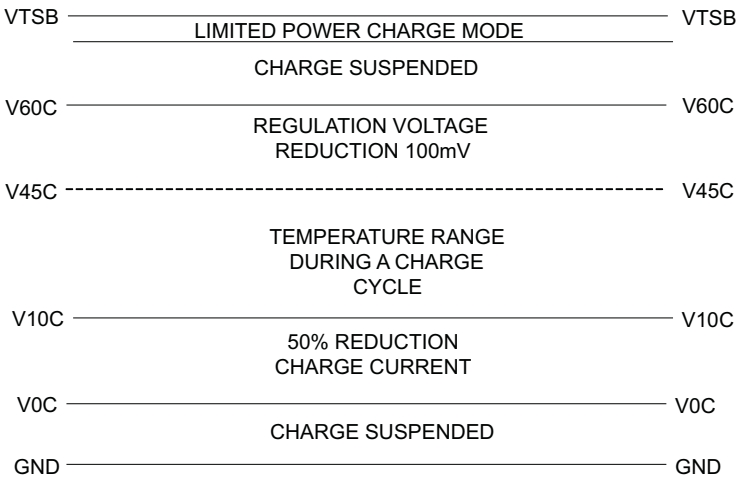


Figure 12. TS Pin, Thermister Sense Thresholds

Assuming a 103AT NTC thermister on the battery pack as shown in Figure 2, the value RT1 can be determined by using the following equation (select the most critical temperature for the best precision):

$$RT1 = \frac{1}{V_{V45C}} \times RTH(45C) - RTH(45C) \quad (1)$$

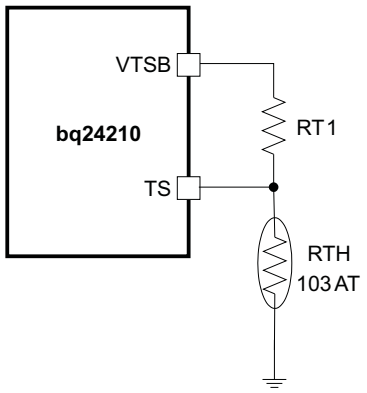


Figure 13. TS Resistor Network

The TS pin has another additional feature. When the TS pin is driven high (V_{TS}> $V_{LP(TS)}$), the IC operates in Limited Power Charge mode.

Limited Power Charge Mode – TS Pin High

When the TS pin goes high to the Limited Power Charge Mode (LPCM) threshold ($V_{LP(TS)}$), the part enters Limited Power Charge mode. This mode is used normally for solar charging applications or other high impedance input sources that desire to modify the termination routine and other timers. When entering the Limited Power Charging mode, the pre-charge timer and 10 hour safety timer is held in reset, and the termination routine is modified. A battery detect routine is run to see if the battery was removed or not. If the battery was removed then the $\overline{CHG}$ pin will go to its high impedance state if not already there. If a battery is detected, the normal charge process begins. If the normal termination conditions are met (Icharge<I_{TERM}, BAT>V_{RCH}) and VBUS_DPM loop is not active, the charging process terminates, and the $\overline{CHG}$ pin goes to its high impedance state if not already there. When the regular timers are disabled there still is a 2 hour timer if the part is stuck in DPM above 4.1 V but outside of termination conditions at which point charging will terminate and re-start if the voltage falls below 4.1V.

When coming out of the Limited Power Charging mode, the battery detect routine is run and if a battery is detected, then a new charge cycle begins and the $\overline{CHG}$ LED turns on.

Limited Power Charge mode is not necessary for all solar charging. A solar panel charging in normal mode without TS pulled high would keep the normal termination timers active and would allow the TS temperature monitoring functions to be used.

If Limited Power Charging mode is not desired upon removal of the battery with a thermister, apply a voltage equal to 30% VTSB on TS pin using two external resistors to set a voltage divider and disable the TS monitor function.

Timers

The pre-charge timer is set to 30 minutes. The pre-charge current is internally set to 20% of the fast charge current.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation or VBUS_DPM. While in thermal regulation or VBUS_DPM, the timer clock slows by a factor of 2, resulting in a clock than counts half as fast which will increase the total time. If either the 30 minute or ten hour timer times out, the charging is terminated and the $\overline{CHG}$ pin goes high impedance if not already in that state. The timer is reset by disabling the IC, cycling power, or going into and out of LPCM.

Termination

Once the BAT pin goes above VRCH (reaches voltage regulation), and the current tapers down to the termination threshold, the $\overline{CHG}$ pin goes high impedance, and a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present, the charge current will terminate. If the battery was removed along with the thermister, then the TS pin is driven high and the charger enters LPCM. If the battery was removed and the TS pin is held in the active region, then the battery detect routine will continue until a battery is inserted.

Battery Detect Routine

The battery detect routine checks for a missing battery while keeping the BAT pin at a useable voltage. Whenever the battery is missing, the $\overline{CHG}$ pin is high impedance.

The battery detect routine is run when entering and exiting LPCM to verify if battery is present, or run all the time if battery is missing. On power-up, if battery voltage is greater than V_{RCH} threshold, a battery detect routine is run to determine if a battery is present.

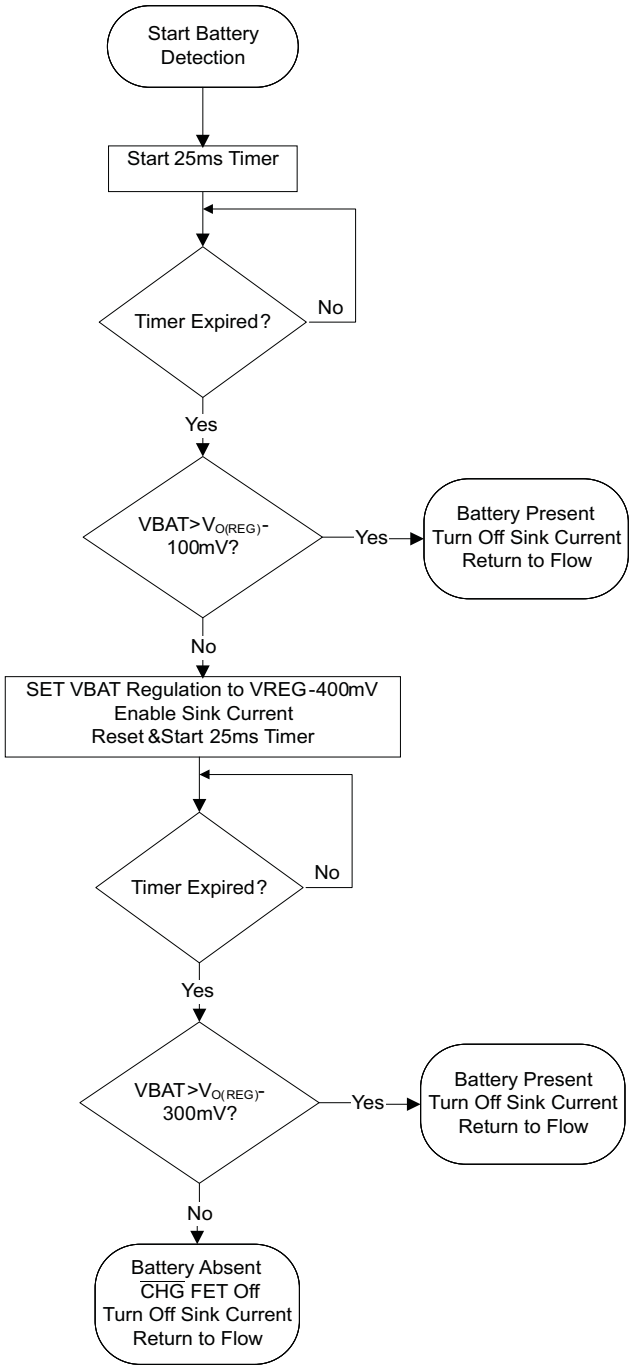


Figure 14. Battery Detection Flow Chart

Refresh Threshold

After termination, if the BAT pin voltage drops to V_{RCH} (100mV below regulation) then a new charge is initiated, but the $\overline{CHG}$ pin remains at a high impedance (off).

Starting a Charge on a Full Battery

The termination threshold is raised by 14%, for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.

Load Mode

Load Mode is used when the charging source is removed and an external accessory needs power from the battery.

To start the Load Mode, the minimum BAT pin voltage is $BAT_{\_REV\_ST}$. When Load Mode is active, the oscillator and charge pump will operate at reduced speed to reduce quiescent current prolonging battery life.

During Load Mode, reverse current is monitored, and once it rises to an internally set threshold, I_{REV_LIMIT}, the load current regulation loop will limit the load current to the threshold for a blanking time of $t_{REV\_LIMIT\_BLK}$. If the over load condition continues after the blanking time of $t_{REV\_LIMIT\_BLK}$, the load current limit threshold will be reduced to $I_{REV\_LIMIT\_BK}$ (about 50mA) and Load Mode continues, until the VBUS drops below UVLO or other failure occurs. If the load current drops below $I_{REV\_LIMIT\_BK}$, the load current limit will be set back to I_{REV_LIMIT} after a delay of $t_{REV\_LIMIT\_REC}$, as shown in Figure 15.

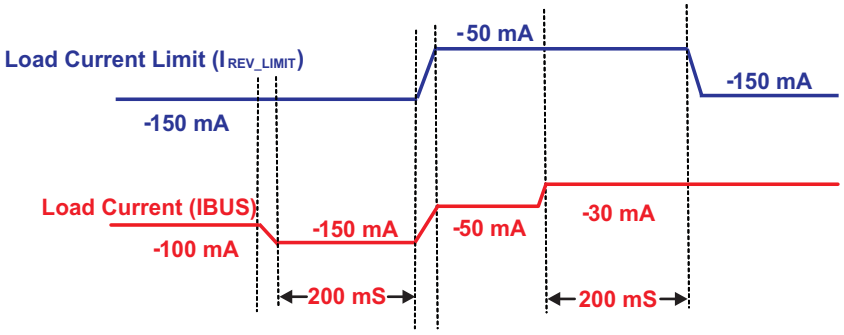


Figure 15. Load Current Limiting

Suspend Mode

When $\overline{EN}$ pin is pulled to HIGH level, the IC operates in Suspend Mode, with Q1 and Q2 OFF and very low leakage current into and between VBUS and BAT pins. The PG pin continues to operate to indicate a good power source even while in suspend mode.

REVISION HISTORY

Changes from Original (December 2010) to Revision A **Page**

- Changed from Product Preview to Production Data 1
- Added sentence to last paragraph of Description (continued) 2
- Changed VBUS description in PIN FUNCTIONS table 2
- Changed Figure 2 3
- Added values to the Thermal Information table 4
- Changed titles in Figure 9 and Figure 10 15
- Changed paragraph under Load Mode section 19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ24210DQCR	ACTIVE	WSON	DQC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24210DQCT	ACTIVE	WSON	DQC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

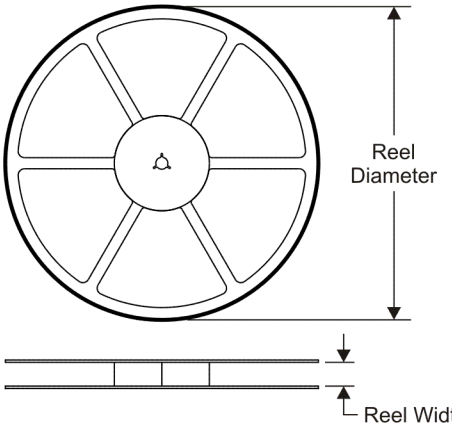
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

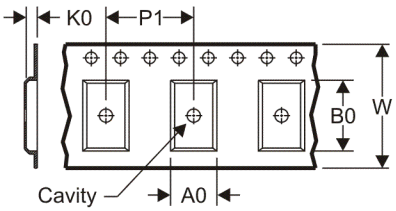
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

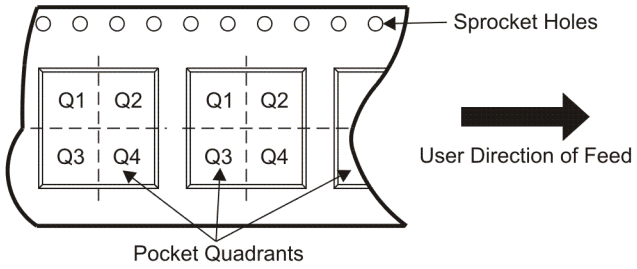


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

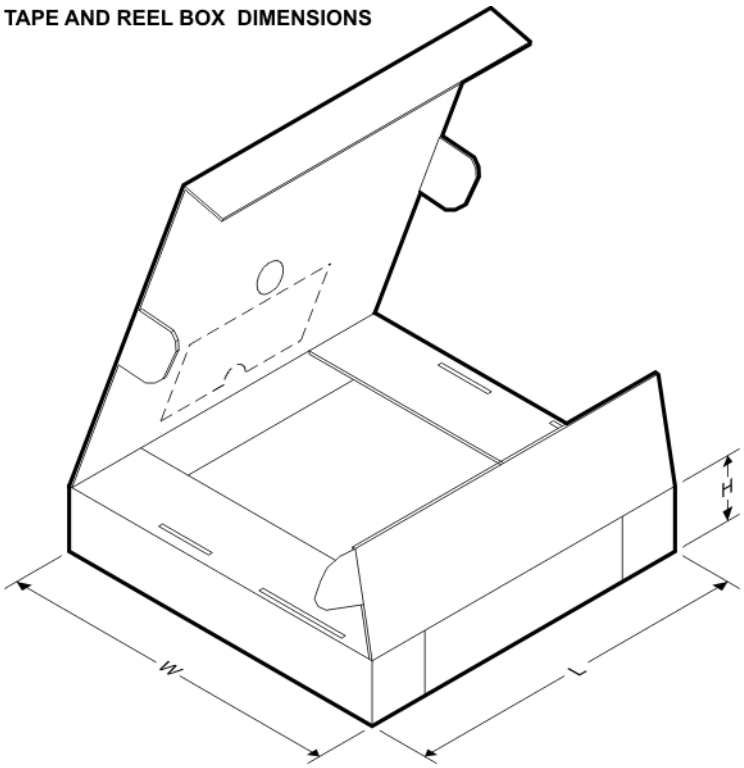
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24210DQCR	WSON	DQC	10	3000	330.0	12.4	2.3	3.3	0.85	4.0	12.0	Q1
BQ24210DQCT	WSON	DQC	10	250	180.0	12.4	2.3	3.3	0.85	4.0	12.0	Q1

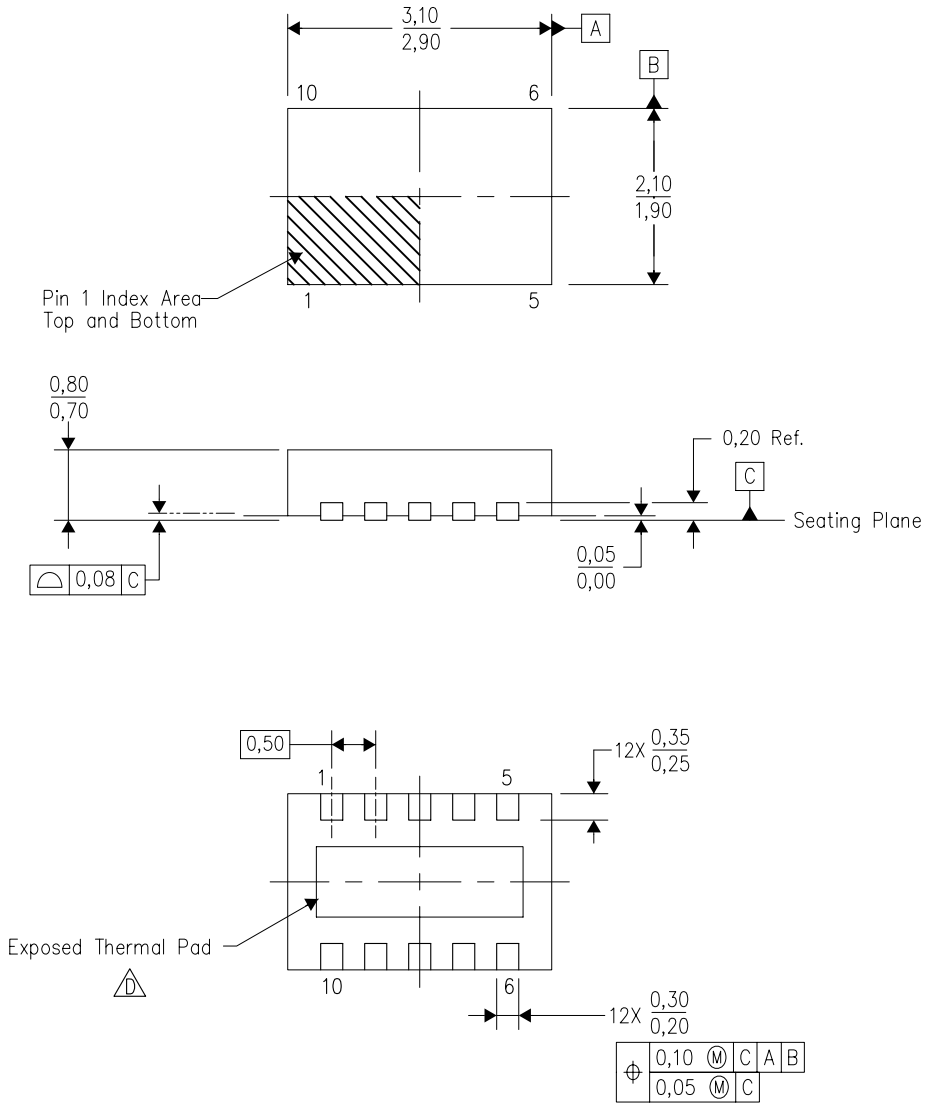
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24210DQCR	WSON	DQC	10	3000	346.0	346.0	29.0
BQ24210DQCT	WSON	DQC	10	250	190.5	212.7	31.8

DQC (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

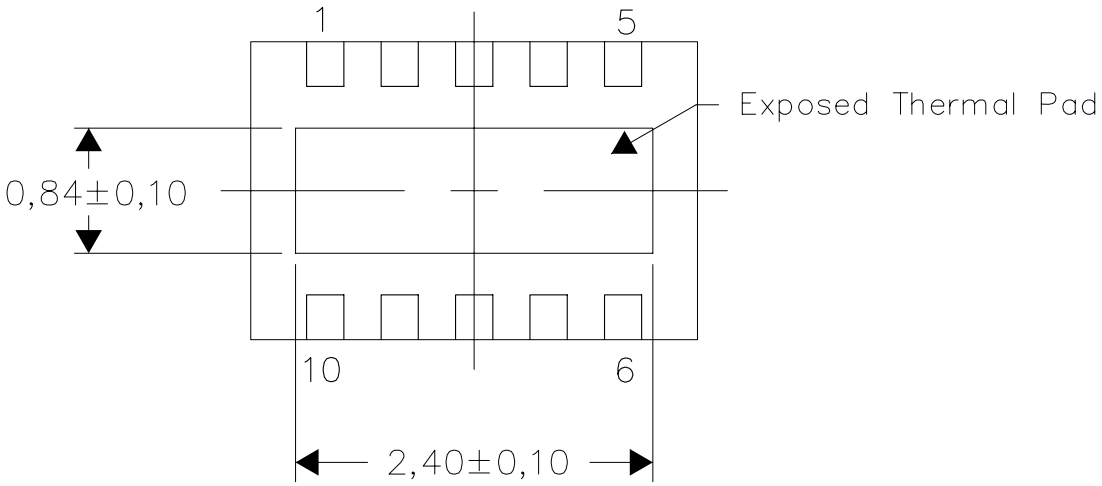
DQC (R–PWSON–N10) PLASTIC SAMLL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209909/B 10/10

NOTE: A. All linear dimensions are in millimeters

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